What is Claimed is:

1. A code generating apparatus, comprising:

a first code generator generating a first code of n symbols;

a second code generator generating a second code of m symbols, where m is greater than n; and

a combiner for combining the symbols generated by the first and second code generators to generate a combined code from which both the first and second codes can be detected.

2. The code generating apparatus of claim 1, wherein the combiner is a multiplexer that interleaves the symbols of the first and second codes to generate an interleaved code.

3. The code generating apparatus of claim 2, wherein n and m are mutually prime.

4. The code generating apparatus of claim 3, wherein m=n+1.

5. The code generating apparatus of claim 1, wherein the first and second codes are pseudonoise codes.

6. The code generating apparatus of claim 2, wherein the multiplexer interleaves the symbols of the first and second codes in a chip by chip manner, and wherein the symbols are comprised of chips.

7. The code generating apparatus of claim 1, wherein the combiner is coupled to the first and second code generators.

8. The code generating apparatus of claim 1, wherein each symbol represents a binary value.

9. A method of generating a combined code comprising:

a) combining a plurality of codes each having a length shorter than the transmission code; and

b) outputting the combined code,

wherein the plurality of codes can be detected from the combined code, and the phase of the combined code can be detected from the plurality of codes.

10. The method of generating a combined code according to claim 9, wherein the plurality of codes is comprised of three codes having lengths m, n and p, where m, n and p are mutually prime.

11. The method of generating a combined code according to claim 10, wherein the combined code has a length of 3•n•m•p.

12. The method of generating a combined code according to claim 10, wherein symbols of the plurality of codes are interleaved.

13. A method of generating a code, comprising:

a) generating a symbol of a first code of length n symbols;

b) generating a symbol of a second code of length m symbols, where m is greater than n; and

c) generating a third code by outputting the symbol of the first code followed by the symbol of the second code.

14. The method of generating a code according to claim 13, wherein n and m are mutually prime.

15. The method of generating a code according to claim 14, wherein m=n+1.

16. The method of generating a code according to claim 13, wherein the first and second codes are pseudonoise codes.

17. The method of generating a code according to claim 13, further comprising,

d) repeating a) through c) at least 2•n•m times.

18. The method of generating a code according to claim 17, wherein in a) the symbols of the first code are generated in order, modulo n, and in b) the symbols of the second code are generated in order, modulo m.

19. The method of generating a code according to claim 13, further comprising,

d) repeating a) through c) a predetermined number of times less than 2•n•m times; and

e) outputting an output signal having a predetermined number of symbols less than 2•n•m symbols.

20. The method of generating a code according to claim 13, wherein each symbol is comprised of chips representing a binary value.

21. A transmitter, comprising:

a controller outputting first, second and third control signals based on a count;

a first code generator generating a first code of n symbols in response to the first control signal;

a second code generator generating a second code of m symbols in response to the second control signal; and

a combiner coupled to the controller and the first and second code generators, wherein the combiner combines the symbols of the first code with the symbols of the second code in response to the third control signal and outputs a combined code.

22. The transmitter according to claim 21, wherein the combiner is a multiplexer for interleaving symbols of the first code with symbols of the second code, thereby generating the combined code as an interleaved code.

23. The transmitter according to claim 21, wherein n and m are mutually prime.

24. The transmitter according to claim 23, wherein m=n+1.

25. The transmitter according to claim 23, wherein the first and second codes are pseudonoise codes.

26. The transmitter according to claim 23, wherein the symbols of the first code are generated in order, modulo n, and the symbols of the second code are generated in order, modulo m.

27. The transmitter according to claim 23, wherein the controller outputs a signal to the multiplexer to output only selected portions of one or more of the first and second codes, so that the interleaved code has a length less than 2•n•m symbols.

28. A transmission signal having a sequence of symbols, the sequence comprising symbols of a first code of n symbols interleaved with symbols of a second code of m symbols.

29. The transmission signal of claim 28, wherein the symbols of the first code are interleaved with the symbols of the second code in a symbol by symbol manner.

30. The transmission signal of claim 28, wherein n and m are mutually prime.

31. The transmission signal of claim 30, wherein m=n+1.

32. The transmission signal of claim 28, wherein the first and second codes are pseudonoise codes.

33. The transmission signal of claim 28, wherein the first code repeats modulo n and the second code repeats modulo m, and the sequence repeats modulo 2•n•m.

34. The transmission signal of claim 28, wherein each symbol is comprised of chips that each represents a binary value.